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**APPLICATION FOR LETTERS PATENT**

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**INTEGRATED CIRCUIT DEVICE,  
SYNCHRONOUS-LINK DYNAMIC RANDOM  
ACCESS MEMORY DEVICE, METHOD OF  
FORMING AN INTEGRATED CIRCUIT DEVICE  
AND METHOD OF FORMING A SYNCHRONOUS-  
LINK DYNAMIC RANDOM ACCESS MEMORY  
EDGE-MOUNTED DEVICE**

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INTEGRATED CIRCUIT DEVICE, SYNCHRONOUS-LINK DYNAMIC  
RANDOM ACCESS MEMORY DEVICE, METHOD OF FORMING  
AN INTEGRATED CIRCUIT DEVICE AND METHOD OF FORMING  
A SYNCHRONOUS-LINK DYNAMIC RANDOM ACCESS MEMORY  
EDGE-MOUNTED DEVICE

TECHNICAL FIELD

The present invention relates to integrated circuit devices, synchronous-link dynamic random access memory devices, methods of forming an integrated circuit device and methods of forming a synchronous-link dynamic random access memory edge-mounted device.

BACKGROUND OF THE INVENTION

Personal computers have experienced expansive growth and improvements in technology in recent decades. Improvements in processing technologies have enabled fabrication of computer components having reduced feature sizes. Such reduction in feature sizes has also enabled the fabrication of smaller components with increased capabilities.

For example, both the operational speeds of processing devices and the capacity to store data of memory devices have been significantly increased. However, there exists a desire to increase the storage capacity of conventional memory devices. Data is stored in components comprising random access memory (RAM) in some conventional configurations. Exemplary random access memory devices include static random access memory (SRAM) and dynamic random access memory (DRAM). It has been desired to increase the speed of memory devices

1 to increase the overall performance of the conventional computer  
2 systems.

3 Synchronous-link dynamic random access memory (SLDRAM)  
4 devices have been introduced to provide faster electronic storage devices.  
5 The synchronous-link dynamic random access memory devices provide  
6 benefits of very high speed (e.g., 400 megahertz data rate) and very  
7 high bandwidth (e.g., 800 Mb/s I/O bandwidth). In addition, such  
8 storage devices can provide pipelined or concurrent operation.  
9 Exemplary synchronous-link dynamic random access memory devices  
10 provide synchronous and packet oriented operation with storage  
11 capabilities in excess of 75 MB.

12 Various packaging configurations have been utilized as housings for  
13 conventional synchronous-link dynamic random access memory devices.  
14 Exemplary configurations include vertical surface mounted packages  
15 (VSMP) and horizontal surface mounted packages (HSMP). In typical  
16 configurations, the leads extend from one surface of the mounted  
17 packages and are bent and trimmed for the desired orientation.

18 It has been observed that conventional synchronous-link dynamic  
19 random access memory devices produce a considerable amount of heat.  
20 Accordingly, various structures have been utilized to reduce or dissipate  
21 the generated heat. One prior art technique has considered the  
22 utilization of a heat sink bonded to an external wall of a package  
23 which houses the synchronous-link dynamic random access memory  
24 semiconductor die. In such conventional designs, an epoxy or other

1 adhesive is typically utilized to bond or otherwise adhere the heat sink  
2 to the external surface of the housing package. Drawbacks are  
3 presented by the conventional designs inasmuch as subsequent processing  
4 of an individual synchronous-link dynamic random access memory device  
5 often results in heating the memory device to the point of failure of  
6 the epoxy heat sink bond.

7 Therefore, there exists a need to provide improved memory  
8 configurations to overcome the shortcomings experienced within the prior  
9 art devices.

### 10 11 SUMMARY OF THE INVENTION

12 The present invention includes integrated circuit devices,  
13 synchronous-link dynamic random access memory devices, methods of  
14 forming an integrated circuit device and methods of forming a  
15 synchronous-link dynamic random access memory edge-mounted device.

16 According to one aspect of the present invention, an integrated  
17 circuit device includes a semiconductor die and a first housing  
18 encapsulating the semiconductor die. A heat sink is positioned  
19 proximate the first housing. A second housing is formed to encapsulate  
20 at least a portion of the heat sink. The heat sink is preferably  
21 thermally coupled with the semiconductor die and configured to dissipate  
22 or expel heat therefrom. The second housing is configured to  
23 encapsulate both the heat sink and the first housing in certain aspects  
24 of the invention.

1 Another aspect of the present invention provides an integrated  
2 circuit device which includes a first housing formed about a  
3 semiconductor die and at least portions of a plurality of leads  
4 electrically coupled with the semiconductor die. A heat sink is  
5 thermally coupled with the first housing. A second housing is formed  
6 about the heat sink and at least a portion of the first housing.

7 The present invention additionally provides methods of forming an  
8 integrated circuit device. One aspect provides a method including the  
9 steps of providing a semiconductor die and forming a first housing  
10 about the semiconductor die. The method also includes thermally  
11 coupling a heat sink with the first housing and forming a second  
12 housing about at least a portion of the heat sink following the  
13 thermally coupling.

14 The present invention also provides additional structure and  
15 methodology aspects.

### 16 17 BRIEF DESCRIPTION OF THE DRAWINGS

18 Preferred embodiments of the invention are described below with  
19 reference to the following accompanying drawings.

20 Fig. 1 is an isometric view of a vertical surface mounted package  
21 in accordance with the present invention.

22 Fig. 2 is a side elevational view of a horizontal surface mounted  
23 package of the present invention.

24 Fig. 3 is a top view of a strip of a plurality of first lead frames.

1 Fig. 4 is a top view illustrating details of one first lead frame of  
2 the strip of Fig. 3.

3 Fig. 5 is an illustrative representation of an exemplary fabrication  
4 step of an integrated circuit device.

5 Fig. 6 is an illustrative representation of another exemplary  
6 processing step subsequent to the step shown in Fig. 5.

7 Fig. 7 is a side elevational view of an integrated circuit package  
8 at an intermediate processing step.

9 Fig. 8 is a top view of a second lead frame.

10 Fig. 9 is a side elevational view of a heat sink of the second  
11 lead frame positioned adjacent a first housing.

12 Fig. 10 is a side elevational view of an integrated circuit device  
13 according to a first embodiment of the present invention.

14 Fig. 11 is a side elevational view of an integrated circuit device  
15 according to a second embodiment of the present invention.

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17 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

18 This disclosure of the invention is submitted in furtherance of the  
19 constitutional purposes of the U.S. Patent Laws "to promote the  
20 progress of science and useful arts" (Article 1, Section 8).

21 Referring to Fig. 1, an integrated circuit device 10 according to  
22 the present invention is illustrated. The described embodiment discloses  
23 a synchronous-link dynamic random access memory (SLDRAM) edge-  
24 mounted device. The depicted integrated circuit device 10 comprises a

vertical surface mounted package (VSMP). A horizontal surface mounted package (HSMP) is also provided in other embodiments. The embodiments depicted herein are exemplary. The present invention is not limited to such disclosed arrangements but can be utilized with other integrated circuit device configurations.

The illustrated integrated circuit device 10 includes a housing 11 provided about an internal semiconductor die 15 and a heat sink 17. As described below with reference to Fig. 2, housing 11 can include a first housing portion and second housing portion (only the second housing portion is visible in Fig. 1). In accordance with the presently described embodiment, semiconductor die 15 comprises synchronous-link dynamic random access memory circuitry. Semiconductor die 15 can be configured to provide additional and/or other functions.

A plurality of leads are coupled with one end of housing 11. In particular, the illustrated leads comprise plural first leads 14 coupled with the internal semiconductor die 15 and plural second leads 16 coupled with heat sink 17. First leads 14 are operable to provide electrical interconnection of semiconductor die 15 with external circuitry (not shown). Second leads 16 are operable to expel, dissipate or otherwise conduct heat generated within integrated circuit device 10 to external components, such as an externally provided heat sink (not shown). First leads 14 and second leads 16 are arranged to provide an integrated circuit device configuration which can be mounted in a vertical orientation.

Referring to Fig. 2, another configuration of integrated circuit device 10a is shown. Like numerals represent like components with any significant differences therebetween being represented by the suffix "a." Integrated circuit device 10a is configured as a horizontal surface mounted package. Similar to the vertical surface mounted package depicted in Fig. 1, integrated circuit device 10a is configured to house semiconductor die 15 and heat sink 17.

First and second leads 14a, 16a are bent or otherwise configured to provide horizontal mounting of integrated circuit device 10a. Leads 14a are configured to provide electrical connection with external electrical couplings (not shown). Second leads 16a are configured to provide coupling of internal heat sink 17 with an external thermal conductor (not shown).

Housing 11 can comprise the same housing configuration in both devices depicted in Fig. 1 and Fig. 2. The depicted housing 11 includes a first housing portion 12 and a second housing portion 13. First housing portion, also referred to as a first housing 12, is formed about semiconductor die 15 and at least a portion of first leads 14a. Second housing portion, also referred to as a second housing 13, is formed about at least a portion of heat sink 17 and at least a portion of second leads 16a.

More specifically, first housing 12 is configured to encapsulate or otherwise house semiconductor die 15 and at least a portion of first leads 14a in the illustrated embodiment. Second housing 13 is



1 configured to encapsulate or otherwise house heat sink 17, first  
2 housing 12 and at least a portion of second leads 16. Second  
3 housing 13 also encapsulates at least a portion of first leads 14 in the  
4 depicted embodiment.

5 Referring to Fig. 3 - Fig. 6, exemplary process steps for  
6 fabrication of first housing 12 are illustrated. Other and/or additional  
7 process steps can be utilized to fabricate first housing 12 of integrated  
8 device 10 in accordance with other fabrication methodologies.

9 Referring specifically to Fig. 3, a lead frame strip 20 is  
10 diagrammatically and in broad outline illustrated. Lead frame strip 20  
11 comprises a plurality of first lead frames 22 provided thereon. First  
12 lead frames 22 are individually configured to couple with and support  
13 a semiconductor die. First lead frames 22 can comprise a thin  
14 conductive metal such as copper. Lead frame strip 20 is utilized to  
15 simultaneously fabricate a plurality of integrated circuit devices.

16 Referring to Fig. 4, details of an exemplary first lead frame 22  
17 are illustrated. Semiconductor die 15 is illustrated coupled with first  
18 lead frame 22 in Fig. 4. In the described embodiment, first lead  
19 frame 22 includes plural first leads 14 operable to provide electrical  
20 connection with semiconductor die 15.

21 First lead frame 22 additionally includes a pad 24 configured to  
22 provide a mounting surface for semiconductor die 15 (a portion of  
23 pad 24 is provided below semiconductor die 15 and is not visible in the  
24 depicted arrangement). Semiconductor die 15 can be mechanically

1 bonded to pad 24 using an epoxy. Other attachment methods of  
2 semiconductor die 15 can be utilized. Pad 24 is coupled with and  
3 supported by external portions of first lead frame 22 via plural lead  
4 frame supports 26.

5 The depicted semiconductor die 15 includes a plurality of bond  
6 pads 30. Following mechanical bonding or other coupling of  
7 semiconductor die 15 with pad 24 of first lead frame 22, wire bonding  
8 connections 32 are formed to couple individual bond pads 30 with  
9 corresponding first leads 14. Wire bonding connections 32 individually  
10 comprise gold in the described embodiment. Wire bonding  
11 connections 32 are operable to provide electrical coupling of first  
12 leads 14 with respective bond pads 30 and internal circuitry of  
13 semiconductor die 15. Alternative electrical connection methods of  
14 leads 14 and semiconductor die 15 are possible.

15 Referring to Fig. 5 and Fig. 6, additional exemplary fabrication  
16 steps of integrated circuit device 10 are described. As shown in Fig. 5,  
17 first lead frame 22 having semiconductor die 15 mounted thereon is  
18 placed within a mold 40. As illustrated, mold 40 comprises opposing  
19 first and second forms 44, 46. Mold 40 is configured in the described  
20 fabrication method to form first housing 12. In particular, first lead  
21 frame 22 comprising first leads 14 and pad 24 and semiconductor  
22 die 15 are provided intermediate opposing forms 44, 46 of mold 40.  
23 Forms 44, 46 include respective dams 48, 50. Lead frame 22 and  
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1 semiconductor die 15 are preferably aligned with dams 48, 50 as shown  
2 in Fig. 5.

3 Mold 40 also provides a defined volume 41 intermediate  
4 forms 44, 46. A tablet of powdered resin 42 is placed within mold  
5 volume 41 and intermediate forms 44, 46. Resin 42 is inserted within  
6 volume 41 to provide material to form first housing 12 to house  
7 semiconductor die 15. A plunger 43 is positioned adjacent volume 41.  
8 Plunger 43 is operable to move upwardly to force resin 42 toward  
9 semiconductor die 15 and lead frame 22 positioned within mold 40.

10 Referring to Fig. 6, following placement of semiconductor die 15  
11 and lead frame 22 within mold 40, forms 44, 46 are brought together.  
12 Respective dams 48, 50 define an inner chamber 52. Chamber 52 is  
13 configured to define the perimeter of first housing 12. Forms 44, 46  
14 also define a runner 54 intermediate volume 41 and chamber 52.  
15 Volume 41 has been substantially filled with plunger 43 in Fig. 6.  
16 Runner 54 and chamber 52 have been substantially filled with resin 42  
17 in Fig. 6.

18 Lead frame 22 and semiconductor die 15 are aligned within  
19 chamber 52 defined within mold 40. Following closure of forms 44, 46,  
20 mold 40 can be heated to an increased temperature, such as 180° C.  
21 Heating of mold 40 results in melting of resin 42 within the tablet.  
22 Plunger 43 can be utilized to force the melted resin 42 through  
23 runner 54 into chamber 52. The melted resin 42 fills chamber 52 as  
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1 shown. Thereafter, resin 42 is permitted to sufficiently solidify or  
2 otherwise cure within mold 40 to form first housing 12.

3 Referring to Fig. 7, first housing 12 and the first lead frame (not  
4 shown in Fig. 7) are removed from the mold following sufficient  
5 solidification of resin 42. As shown, resin 42 encapsulates  
6 semiconductor die 15, lead frame pad 24, wire bonding connections 32,  
7 and a portion of first leads 14. Unencapsulated portions of first  
8 leads 14 are exposed outside of first housing 12.

9 First housing 12 can be removed from the first lead frame  
10 following removal of first housing 12 and the first lead frame from  
11 mold 40. In particular, pad connections 26 (shown in Fig. 4) are  
12 broken to remove first housing 12. Thereafter, first housing 12 can  
13 undergo further processing to form the desired integrated circuit  
14 device 10.

15 Referring to Fig. 8, a second lead frame 60 is illustrated. Second  
16 lead frame 60 includes heat sink 17. Second lead frame 60 is formed  
17 of a thermally conductive material such as a metal in the described  
18 embodiment. Heat sink 17 includes a body 18. Heat sink body 18 is  
19 supported by plural supports 62. The illustrated heat sink 17 includes  
20 plural second leads 16 coupled with heat sink body 18. Second lead  
21 frame 60 is typically provided within a lead frame strip (not shown)  
22 similar to first lead frame strip 20 shown in Fig. 3. Such a strip could  
23 include a plurality of heat sinks 17 corresponding to the number of first  
24 lead frames 22 provided.

1 Referring to Fig. 9, following sufficient solidification of first  
2 housing 12 and removal thereof from the first mold and the first lead  
3 frame, heat sink 17 of second lead frame 60 is thermally coupled with  
4 first housing 12. In the described embodiment, heat sink 17 is  
5 positioned proximate or adjacent first housing 12. In the preferred  
6 embodiment, heat sink 17 is positioned against or in contacting relation  
7 with first housing 12. Heat sink 17 is configured to draw heat  
8 generated from semiconductor die 15 and preferably expel or dissipate  
9 the heat.

10 The second housing of the integrated circuit device is thereafter  
11 formed. Although not illustrated, the method of forming the first  
12 housing can be utilized to form the second housing. Such can be  
13 referred to as a "double molding" process. More specifically, following  
14 the positioning of heat sink 17 against first housing 12, or other  
15 suitable thermal coupling, second lead frame 60 and first housing 12 are  
16 provided within a second mold. Such a mold contains appropriate  
17 forms having dams to define a second chamber for forming the second  
18 housing of the integrated circuit device.

19 A resin tablet is inserted into the second mold and first  
20 housing 12 and second lead frame 60 are placed within the appropriate  
21 second chamber formed within the second mold. The second mold is  
22 subsequently heated to a sufficient elevated temperature to melt the  
23 resin. Thereafter, a plunger is utilized to force the melted resin into  
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1 the second chamber containing first housing 12 and second lead  
2 frame 60.

3 The resin is thereafter permitted to sufficiently solidify to form  
4 the second housing. First and second housings 12, 13 (shown in  
5 Fig. 10) are removed from the mold following such solidification.  
6 Second housing 13 is then removed from second lead frame 60 by  
7 breaking connections 62 (shown in Fig. 8). Connections 62 are broken  
8 to free heat sink 17 and second housing 13 from lead frame 60.

9 Referring to Fig. 10 and Fig. 11, plural housing  
10 configurations 11, 11a of respective integrated circuit device  
11 configurations 10, 10b are illustrated. Fig. 10 and Fig. 11 individually  
12 illustrate respective integrated circuit devices 10, 10b at a step following  
13 the removal of devices 10, 10b from the second lead frame.  
14 Devices 10, 10b are depicted at a step prior to final fabrication steps  
15 comprising bending and trimming of first leads 14 and second leads 16  
16 which extend from the illustrated housings 11, 11a.

17 Referring specifically to Fig. 10, the first configuration of  
18 housing 11 is shown. First housing 12 of housing 11 is formed about  
19 semiconductor die 15 and at least portions of leads 14 coupled with  
20 semiconductor die 15. Second housing 13 is formed about at least a  
21 portion of first housing 12, at least a portion of first leads 14 and at  
22 least a portion of heat sink 17.

23 In particular, first housing 12 and second housing 13 individually  
24 comprise encapsulant housings in the configuration shown in Fig. 10.

1 More specifically, first housing 12 encapsulates semiconductor die 15 and  
2 at least a portion of first leads 14. Second housing 13 encapsulates a  
3 majority of heat sink 17 and a majority of first housing 12. More  
4 specifically, second housing 13 encapsulates first housing 12, heat sink  
5 body 18, and at least a portion of first leads 14 and second leads 16.

6 Referring specifically to Fig. 11, another configuration of  
7 housing 11a of integrated circuit device 10b is illustrated. In the  
8 depicted configuration, first housing 12 encapsulates semiconductor die 15  
9 and a portion of first leads 14. Second housing 13a is shown provided  
10 about at least a portion of heat sink 17 and first housing 12. In  
11 particular, second housing 13a is shown encapsulating three surfaces of  
12 heat sink body 18 and a portion of first housing 12 in the configuration  
13 depicted in Fig. 11.

14 Other housing configurations of integrated circuit device 10 can  
15 be formed according to the present invention. First housing 12 can be  
16 provided about or configured to encapsulate more or less components  
17 of integrated circuit device 10. Further, more or less portions of first  
18 housing 12 and heat sink 17 can be encapsulated or otherwise covered  
19 by second housing 13.

20 External exposed portions of first leads 14 and second leads 16  
21 can be trimmed and/or bent into appropriate positions to provide the  
22 desired integrated circuit device 10, 10a forming a vertical surface  
23 mounted package or a horizontal surface mounted package as depicted  
24 in Fig. 1 and Fig. 2, respectively.

1 In compliance with the statute, the invention has been described  
2 in language more or less specific as to structural and methodical  
3 features. It is to be understood, however, that the invention is not  
4 limited to the specific features shown and described, since the means  
5 herein disclosed comprise preferred forms of putting the invention into  
6 effect. The invention is, therefore, claimed in any of its forms or  
7 modifications within the proper scope of the appended claims  
8 appropriately interpreted in accordance with the doctrine of equivalents.  
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